AMENDMENTS TO THE CLAIMS:

This listing of claims replaces all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Previously Presented) A method comprising:

storing partial quotients of a continued fraction in a first set of counters;

initializing a second set of counters with counter values;

decrementing a target counter in the second set of counters to obtain a decremented counter value; and

outputting a value that corresponds to a partial quotient in a first counter in the first set of counters, the value being based on the decremented counter value;

wherein the value (ii) comprises part of a clock signal that is used to clock digital circuitry, (ii) is used to correct a clock signal for clocking digital circuitry, (iii) is used to schedule network traffic, or (iv) is used in a computer graphics application.

2. (Original) The method of claim 1, further comprising:

determining the value based on the decremented counter value.

3. (Original) The method of claim 2, wherein determining the value comprises:

determining if the decremented counter value is zero;

assigning the value to be equal to the partial quotient in the first counter if the decremented counter value is not zero; and

assigning the value to be equal to the partial quotient in the first counter plus one if the decremented counter value is zero.

4. (Original) The method of claim 3, wherein if the decremented counter value is zero, the method further comprises:

loading the target counter with a partial quotient from a counter in the first set of counters that corresponds to the target counter.

5. (Original) The method of claim 4, wherein if the decremented counter value is zero, the method further comprises:

incrementing a value in a counter that precedes the target counter in the second set of counters.

6. (Original) The method of claim 5, wherein the value is incremented in a counter that immediately precedes the target counter.

7. (Original) The method of claim 1, further comprising:

decrementing a counter value in a counter that follows the target counter in the second set of counters to obtain a second decremented counter value; and

outputting a value that corresponds to a partial quotient in a first counter, the value being based on the second decremented counter value from the second set of counters.

8. (Original) The method of claim 1, wherein the counters comprise software counters.

9 to 11. (Cancelled)

12. (Currently Amended) An article comprising a machine-readable medium that stores executable instructions that cause a machine to:

store partial quotients of a continued fraction in a first set of counters;

initialize a second set of counters with counter values;

decrement a target counter in the second set of counters to obtain a decremented counter value; and

output a value that corresponds to a partial quotient in a first counter in the first set of counters, the value being based on the decremented counter value;

wherein the value (ii) comprises part of a clock signal that is used to clock digital circuitry, (ii) is used to correct a clock signal for clocking digital circuitry, (iii) is used to schedule network traffic; or (iv) is used in a computer graphics application

13. (Previously Presented) The machine-readable medium of claim 12, further comprising instructions to:

determine the value based on the decremented counter value.

14. (Original) The machine-readable medium of claim 13, wherein determining the value comprises:

determining if the decremented counter value is zero;

assigning the value to be equal to the partial quotient in the first counter if the decremented counter value is not zero; and

assigning the value to be equal to the partial quotient in the first counter plus one if the decremented counter value is zero.

15. (Original) The machine-readable medium of claim 14, wherein the machine-readable medium further comprises instructions to:

load the target counter with a partial quotient from a counter in the first set of counters that corresponds to the target counter if the decremented counter value is zero.

16. (Original) The machine-readable medium of claim 15, wherein the machine-readable medium further comprises instruction to:

increment a value in a counter that precedes the target counter in the second set of counters if the decremented counter value is zero.

17. (Original) The machine-readable medium of claim 16, wherein the value is incremented in a counter that immediately precedes the target counter.

18. (Original) The machine-readable medium of claim 11, further comprising instructions to:

decrement a counter value in a counter that follows the target counter in the second set of counters to obtain a second decremented counter value; and

output a value that corresponds to a partial quotient in a first counter, the value being based on the second decremented counter value from the second set of counters.

19. (Original) The machine-readable medium of claim 11, wherein the counters comprise software counters.

20 to 22. (Cancelled)

23. (Original) An apparatus comprising:

a first set of counters to store partial quotients of a continued fraction;

a second set of counters to store counter values, the second set of counters corresponding to the first set of counters; and

circuitry to decrement a counter value in a target counter in the second set of counters to obtain a decremented counter value, and to output a value that corresponds to a partial quotient in a first counter in the first set of counters, the value being based on the decremented counter value.

24. (Original) The apparatus of claim 23, wherein the circuitry determines the value based on the decremented counter value.

25. (Original) The apparatus of claim 24, wherein determining the value comprises:

determining if the target counter has a counter value of zero;

assigning the value to be equal to the partial quotient in the first counter if the target counter does not have a counter value of zero; and

assigning the value to be equal to the partial quotient in the first counter plus one if the target counter has a counter value of zero.

26. (Original) The apparatus of claim 25, wherein if the target counter has a counter value of zero, the circuitry loads the target counter with a partial quotient from a counter in the first set of counters that corresponds to the target counter.

27. (Original) The apparatus of claim 26, wherein if the target counter has a counter value of zero, the circuitry increments a value in a counter that precedes the target counter in the second set of counters.

28. (Previously Presented) A clock generating circuit comprising:

an oscillator to produce a clock signal;

memory comprising a first set of counters and a second set of counters; and

a controller to:

generate partial quotients of a continued fraction based on the clock signal;

store the partial quotients in a the first set of counters;

store counter values in a the second set of counters;

decrement a counter value in a target counter in the second set of counters to obtain a decremented counter value; and

output a value that corresponds to a partial quotient in a first counter in the first set of counters, the value being based on the decremented counter value;

wherein the value (ii) comprises part of a clock signal that is used to clock digital circuitry, (ii) is used to correct a clock signal for clocking digital circuitry, (iii) is used to schedule network traffic, or (iv) is used in a computer graphics application

29. (Cancelled)

30. (Previously Presented) The clock generating circuit of claim 28, wherein the controller is configured to:

determine if the decremented counter value is zero;

assign the value to be equal to the partial quotient in the first counter if the decremented counter value is not zero; and

assign the value to be equal to the partial quotient in the first counter plus one if the decremented counter value is zero.